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Oblon, Spivak, McClelland, Maier & Neustadt
4Th Floor
1755 Jefferson Davis Highway
ARLINGTON, VA 22202

EXAMINER	
CHAN, ALEX H	

ART UNIT	PAPER NUMBER
2633	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/594,556	WADA ET AL.	
	Examiner	Art Unit	
	Alex H Chan	2633	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 June 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 June 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings are objected to because there is an apparent spelling error for:

a. Reference number 2d of Fig. 2 and 84 of Fig. 11(a) describe respective "optical encader" and "optical encorder" where "optical encoder" might have been intended.

b. "Intesity" of Fig. 5 is described where "intensity" might have been intended.

c. Reference number 141c of Fig. 14 describes "controler" where "controller" might have been intended.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. **Claims 13-17** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In particular, each of the above recited claims fails to depend appropriately on its corresponding claim. For example, claims 13-17 recite a packet router according to claim 11 when the elements and limitations lack antecedent basis. However, claims will be evaluated with merits by examiner's assumption that all claims 13-17 depend on independent claim 12.

4. **Claims 11 and 17** have the term "at a portion where it is desired" is a relative term which renders the claim indefinite. The term "at a portion where it is desired" is not defined by the

claim, the specification (p. 13, lines 23-33) does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claims 1, 4, 7, 10 and 12** are rejected under 35 U.S.C. 103(a) as being unpatentable over Araki in view of U.S. patent No. 5,729,548 to Holender.

Regarding claim 1, Araki discloses a photonic network packet routing method (Fig. 1 or Fig. 20) comprising a step of discriminating (e.g. extracting) the encoded address information of the IP packet (Col. 12, lines 33-36) by optical correlation processing (e.g. via 105, 107, 109 and 110 of Fig. 2 and via 503 and 525 of Fig. 11), a step of switching to an output path (e.g. via combination of 103, 104 and 100 of Fig. 1) for the IP packet based on a result of the discrimination (e.g. via 1003 and 1004 of Fig. 2 and Col. 12, lines 37-50), and a step of outputting the IP packet labeled with prescribed address information (e.g. Destination 1 of input unit of Fig. 25 and 2003 of Fig. 24 and Col. 11, lines 37-44) on the output path selected by the switching step (Col. 10, lines 39-47 and Col. 11, lines 11-21). Though he discloses a step of encoding address information (e.g. 950 of Fig. 30) using light attributes (1001 of Fig. 30), he fails to disclose a step of optically encoding destination address information attached to an IP packet. Holender discloses an optical encoder (optically encoding) (916 of Fig. 9) for encoding

optical pattern that corresponds to the destination's address (destination address information) (Col. 2, lines 24-52 and Col. 15, lines 39-48) attached with packet payload (913 of Fig. 9) and packet address (912 of Fig. 9). Accordingly, one of the ordinary in the art would have been motivated to incorporate an optical encoder for optically encoding address information to increase the speed of telecommunications switches by adapting optical encoding-decoding techniques to telecommunications applications. Therefore, it would have been obvious to one of artisan skill in the art to have modified the optical packet switching system of Araki by substituting the steps of encoding address information with steps of encoding address information using optical encoders as taught by Holender to obtain the invention as claimed in claim 1.

Regarding claim 4, Araki in view of Holender discloses discrimination of the optically encoded address information (e.g. via 916 of Fig. 9, Holender) is conducted by sending the IP packet (e.g. 1001 of Fig. 11, Araki) labeled with address information (e.g. via 1003 or 525 or 1002 of Fig. 11, Araki or via 912 of Fig. 9, Holender) onto a number of arms equal to the number of address (e.g. one address is extracted from the packet which is sent to one arm) entries (outputs of 101-1 to 101-4 of Fig. 11 are sent via 100 to corresponding output unit 502-1 to 502-4 of Fig. 11, Araki) and simultaneously conducting optical correlation processing (e.g. via 105, 107, 109 and 110 of Fig. 2 and via 503 and 525 of Fig. 11, Araki) on all arms in parallel.

Regarding claim 7, Araki in view of Holender discloses dividing an IP packet having encoded address information (e.g. 1001 of Fig. 2 or Fig. 6, Araki) in two (e.g. one part directs to 107 and the other to 109 of Fig. 2, Araki), a step of conducting optical correlation processing (e.g. via 105, 107, 109 and 110 of Fig. 2 and via 503 and 525 of Fig. 11, Araki) to discriminate

(e.g. decode) address information from an optical code in one IP packet containing address information (e.g. via 1003 of Fig. 2 or 116 of Fig. 4 and Col. 13, lines 14-18, Araki) between the two divided IP packets, a step of selecting an output path (e.g. via selector, 108 of Fig. 2 or 121, 1008 and 1009 of Fig. 4, Araki) based on a result of the discrimination (e.g. 1005 of Fig. 2 and Col. 12, lines 40-46 or e.g. base on contention resolution, Col. 13, lines 19-44, Araki), and a step of outputting the other divided IP packet on the selected output path (e.g. 1002 of Fig. 2 switches via 100 of Fig. 1 to the output port which corresponds to its address or via 1008-1 to output unit 1 while 1005-1 goes to input unit 1, Fig. 4, Araki).

Regarding claim 10, Araki in view of Holender discloses all limitations as discussed above, further discloses an optical switch of a prescribed output path (e.g. via optical gate 874 of Fig. 22, Araki) is turned ON by the discriminated optical signal (e.g. if the higher bits are "0", Col. 27, lines 11-27, Araki).

Regarding claim 12, Araki discloses all limitations as discussed in claim 1, further discloses branching means (e.g. via 105 of Fig. 2) for sending the IP packet having the encoded destination address information onto two paths (e.g. send 1001 to 107 and 109 of Fig. 2), address processing means (e.g. via 1003 and 1004 of Fig. 2 or via contention resolution circuit, Fig. 4) for subjecting one IP packet received from the branching means (105 of Fig. 2) to optical correlation processing (e.g. via 105, 107, 109 and 110 of Fig. 2 and via 503 and 525 of Fig. 11) and outputting a switch control signal(e.g. via 1005 of Fig. 2 or output from 104 of Fig. 11) based on a result of the discrimination (e.g. based on contention, Col. 10, lines 57-67); and switch means (e.g. via combination of 103, 104 and 100 of Fig. 1 and 100 of Fig. 5) for selectively outputting the packet (e.g. via 108 of Fig. 2) by switching an output path of the other

packet (1002 of Fig. 2) received from the branching means based on the address control signal (1005 of Fig. 2) from the address processing means.

7. **Claims 2-3 and 5** are rejected under 35 U.S.C. 103(a) as being unpatentable over Araki in view of Holender as applied to claim 1, and further in view of U.S. Patent No. 6,473,214 B1 to Roberts et al (hereinafter Roberts).

Regarding claim 2, Araki in view of Holender discloses all limitations as discussed above, further discloses the optical encoding (e.g. via 916 of Fig. 9, Holender) is conducted by dividing an optical pulse output (e.g. via 873 of Fig. 22, Araki) by a pulse source (e.g. via 871 of Fig. 22 and Col. 5, lines 50-53, Araki) into N number of chip pulses ($N \geq 2$) (Col. 5, lines 61-67, Araki) and recombining (e.g. via 875 of Fig. 22, Araki) the divided optical chip pulses. He fails to discloses an optical encoding having a prescribed delay time therebetween, imparting the individual chip pulses with phase shifts of "0" or "π'" relative to a light carrier phase of the chip pulses. Roberts discloses an optical encoder (10 of Fig. 1) having a prescribed delay time therebetween (e.g. via 58 of Fig. 5 and Col. 12, lines 57-60), imparting the individual chip pulses with phase shifts of "0" or "π'" (e.g. by producing zero or +/- π phase difference) relative to the signals being combined (light carrier phase of the chip pulses) (Col. 9, lines 5-14). Accordingly, one of the ordinary in the art would have been motivated to incorporate the above delays and phase shift for producing maximum constructive and destructive interference, which could facilitate the optical signal transmission of high speed signals over long distances, with relatively low technical complexity and cost (Col. 2, lines 66-67 & Col. 3, lines 1-3). Therefore, it would have been obvious to one of artisan skill in the art to have modified the optical packet switching system of Araki in view of Holender by prescribing a delay time and imparting the individual

chip pulse with phase shifts of "0" or "π"' in the process of optical encoding because Roberts suggests that this would produce maximum constructive and destructive interference.

Regarding claim 3, Araki in view of Holender and Roberts discloses all limitations as claimed in claim 2, further discloses an optical encoding (e.g. via 916 of Fig. 9, Holender) is conducted by changing normalized intensity (e.g. via amplitude modulation, Col. 1, lines 35-40, Roberts) of the individual chip pulses to "1" or "0" (e.g. amplitude modulation enables recovery of binary signal, Col. 3, lines 39-44, Col. 4, lines 55-65 & Col. 13, lines 45-60, Roberts). Also, it is extremely well known and conventional to change the optical intensity of pulses to 1s and 0s for encoding purposes, such as NRZ and RZ format encoding.

Regarding claim 5, Araki in view of Holender and Roberts discloses discrimination of the encoded address information (e.g. via 916 of Fig. 9, Holender) is conducted by subjecting optical chip pulses to matched filtering (e.g. via. 20 or 24 of Fig. 1, Roberts), effecting threshold processing on a center peak value (e.g. by having passband centered on the desired frequency or any desired frequency range, Col. 9, lines 51-60, Roberts) of a generated autocorrelation function (Fig. 6, Roberts), and optically regenerating the obtained "0" or "1" (e.g. maximum optical signal amplitude represents a "0" bit and a minimum optical signal amplitude represents a "1" bit, Col. 9, lines 61-67, Roberts or).

8. **Claims 6 and 8** are rejected under 35 U.S.C. 103(a) as being unpatentable over Araki in view of Holender as applied to claim 1, and further in view of U.S. Patent No. 6,160,656 to Mossberg et al (hereinafter Mossberg).

Regarding claim 6, Araki discloses a packet router comprising a step of optical decoding but fails to disclose that it comprises of a step of subjecting an output of an optical decoder to

time gate processing, when subjecting a center peak value of a correlation function to threshold processing, thereby cutting off a center part and eliminating side-lopes of correlation waveform and a step of conducting threshold processing. Mossberg teaches the output of grating (optical decoder) (21 of Fig. 2a & Col. 4, lines 11-14) is subject to be detected by time-integrating linear or nonlinear device (time gate processing) (24a and 24b of Fig. 2a or 29a and 29b of Fig. 2b and Col. 4, lines 14-17), when subjecting a center peak value of a correlation function (e.g. 23 of Fig. 2a) to threshold processing (e.g. via threshold detection, Col. 2, lines 5-13 or via electronic thresholding device Col. 3, lines 30-34 or via by emitting a signal that is in the form of a short auto-correlation pulse, Col. 4, lines 7-45), thereby cutting off a center part and eliminating side-lopes of correlation waveform (e.g. 28 of Fig. 2b) and a step of conducting threshold processing (e.g. by setting a threshold level to discriminate between optical signals of similar energy but with and without high power subsignals, Col. 4, lines 43-64). Accordingly, one of ordinary skill in the art would have been motivated to subject the output of grating in the form of an optical decoder to time gate and threshold processing to provide a means of processing output channel signals so as to provide a robust means of differentiating between output signals of similar energy but different temporal waveform without the need of time-solving the waveform of the output signals (Col. 1, lines 60-65). Therefore, it would have been obvious to a person of ordinary skill in the art to have modified the optical packet switching system of Araki in view of Holender by substituting the grating with an optical decoder which subjects its output to time gate and threshold processing to obtain the invention as specified in claim 6.

Regarding claim 8, Araki in view of Holender and Mossberg discloses the address information (e.g. via 912 and 916 of Fig. 9, Holender) is discriminated by sending the IP packet

(e.g. 1001 of Fig. 11, Araki) onto a number of arms equal to the number of output paths (e.g. one address is extracted from the packet which is sent to one arm) entries (e.g. outputs of 101-1 to 101-4 of Fig. 11 are sent via 100 to corresponding output unit 502-1 to 502-4 of Fig. 11, Araki) and simultaneously conducting optical correlation processing (e.g. via 105, 107, 109 and 110 of Fig. 2 and via 503 and 525 of Fig. 11, Araki) on all arms in parallel.

9. **Claim 9** is rejected under 35 U.S.C. 103(a) as being unpatentable over Araki in view of Holender as applied to claim 7, and further in view of U.S. Patent No. 6,128,115 to Shiragaki.

Regarding claim 9, Araki in view of Holender discloses an optical code in the one packet (e.g. 912 and 916 of Fig. 9, Holender) that is discriminated by optical correlation processing but he fails to disclose the discriminated signal is converted to an electric signal, and a gate of a prescribed output path is opened by the electric signal. Shiragaki discloses a wavelength converter having gate switch function (i.e. gate), for converting the optical signal (discriminated signal) to an electric signal where the electric switch is added for performing gate operation (Col. 11, lines 28-39) (e.g. such operations include switching the mode for outputting the light and mode not for outputting the light, Col. 2, lines 57-60). Accordingly, one of the ordinary would have been motivated to convert the optical signal into electric where the electric signal opens the gate of an output path to provide a gate switch having space switch and wavelength switch section integrated whereby packaging volume and cost are thus reduced (Col. 2, lines 37-41). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the optical packet switching system of Araki in view of Holender by substituting the optical gate (e.g. 874 of Fig. 22) with a method that converts the discriminated signal to electric signal and a gate of prescribed output path is opened

by the electric signal because Shiragaki suggests that this would reduce the packing volume and cost when both switch and wavelength sections are integrated.

10. **Claims 11 and 17 (as far as understood)** is rejected under 35 U.S.C. 103(a) as being unpatentable over Araki in view of Holender as applied to claim 1 above, and further in view of U.S. Patent No. 5,365,362 to Gnauck et al (hereinafter Gnauck).

Regarding claim 11, Araki in view of Holender discloses a packet routing method but he fails to disclose a step of combining the IP packet output on the prescribed path and a pulse signal for control adjusted to generate an optical pulse at a portion where it is desired to convert the optical code and a step of converting the combined signal into a prescribed optical code by cross-phase conversion. Gnauck discloses combining (e.g. via beam combiner of Fig. 5) the IP packet output (e.g. output of channel router, 56 of Fig. 5) on the prescribed path and a pulse signal (e.g. pulse signal from pump source which combines with router output at beam combiner, Fig. 5 or 31 of Fig. 4) for control adjusted (Col. 11, lines 59-68 and Col. 12, lines 109) to generate an optical pulse at a portion (e.g. at any part of the fiber according to L & Col. 15, lines 33-35) where it is desired to convert the multi-channel signal having a plurality of channel signals (optical code). and a step of converting (e.g. via phase conjugation, 50 of Fig. 5 or via modulation, Col. 1, lines 51-54) the combined signal into a prescribed phase conjugated output signal (optical code) by four photon mixing (cross-phase conversion). Accordingly, one of ordinary skill in the art would have been motivated to incorporate the above means to achieve substantially higher bit rate distance (Col. 4, lines 42-45), and therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the optical packet switching system of Araki in view of Holender by substituting the above steps

of combining the packet output and pulse signal and a step of converting the combine signal by cross phase modulation to obtain the invention as claimed in claim 11 because Gnauck suggests that this would enable a higher bit rate distance.

Regarding claim 17, Araki in view of Holender and Gnauck discloses all limitations as discussed above in rejecting claim 11, further discloses a combiner (e.g. beam combiner of Fig. 5, Gnauck) and a nonlinear optical medium (e.g. 40 of Fig. 4 and Col. 12, lines 16-18, Gnauck).

11. **Claims 13-16** are rejected under 35 U.S.C. 103(a) as being unpatentable over Araki in view of Holender, and further in view of Roberts.

Regarding claim 13, Araki in view of Holender discloses all limitations as discussed in rejecting claims 1 and 12 above, further discloses tunable taps (optical splitter, 873 of Fig. 22, Araki) and a combiner (875 of Fig. 22, Araki or 52 of Fig. 5). However, he fails to disclose optical phase shifters. Roberts discloses optical delay line (optical phase shifters) (e.g. 58 of Fig. 5 changes phase via delay T, Col. 9, lines 10-14 and Col. 10, lines 16-24, Roberts). One of the ordinary skill in the art would have been motivated to incorporate the optical delay line in the form of optical phase shifters for providing different optical signal frequencies (Col. 12, lines 38-43). Therefore, it would have been obvious to one of artisan skill in the art to have modified the optical packet switching system of Araki by incorporating optical phase shifters in order to obtain the claimed invention as claimed in claim 13.

Regarding claim 14, Araki in view of Roberts discloses all limitations as discussed in 13, further discloses gate switches for changing optical intensity (i.e. amplitudes) of the chip pulses to "1" and "0" (Fig. 28 and Col. 27, lines 11-48, Araki and Col. 3, lines 16-18 and lines 39-41, Roberts).

Regarding claim 15, Araki in view of Roberts discloses all limitations as discussed in claim 13, further discloses a decoder provided on the individual arms for outputting a switch control signal (e.g. via connection request signal) when the decoder's own code and the code of IP packet (e.g. by decoding address of output unit) coincide (e.g. check associated destination) (Col. 13, lines 14-18 and Col. 15, lines 34-52 and Col. 24, lines 31-42, Araki).

Regarding claim 16, Araki in view of Roberts discloses all limitations as discussed in claim 12, further discloses that the switch means comprises means for sending the other IP packet (1002 of Fig. 2, Araki) sent onto the other path by the branching means onto a number of arms equal to the number of output ports (e.g. four light signals 1002 of Fig. 1 from respective input units 101 of Fig. 1 switch accordingly to 4 output units 102 of Fig. 1) and an optical gate (874 of Fig. 22) provided on each arm (Col. 10, lines 39-47, Araki) that opens in response to a switching control signal from the decoder (872 of Fig. 22 and Col. 27, lines 8-10 and lines 49-67) to output the IP packet onto the arm.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Sasayama and Prucnal cited to show packet switching and its method and components such as combiner, switches, encoders, decoders, packet detectors and wavelength converter. Masetti is cited to illustrate photonic switching network having buffers (delay lines), converters, filters and switches. Cotter is cited to show optical processing and electronic processing of an incoming cell or packet, its routing algorithm and components. Dennis is cited to demonstrate an optical router and processor for processing packets. Dantu is cited to show IP router in a optical ring network and a processor for processing packets. Van Der Tolis cited to

show an optical packet switching network having transmitters for transmitting packets with re-assigned addresses and components required for switching. Kim is cited to show optical packet header processing. Hass is cited to illustrate the switching stages of packets via delay lines, detecting means and switching means. Chinn is cited to show na otpical phase controllerof a optical switch. Tayonaka et al is cited to show an optical routing system having optical pulse trains.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alex H Chan whose telephone number is (703) 305-0340. The examiner can normally be reached on Monday to Friday (8am to 6pm EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jason Chan can be reached on (703) 305-4729. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Alex Chan
Patent Examiner
October 15, 2003

JASON CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600